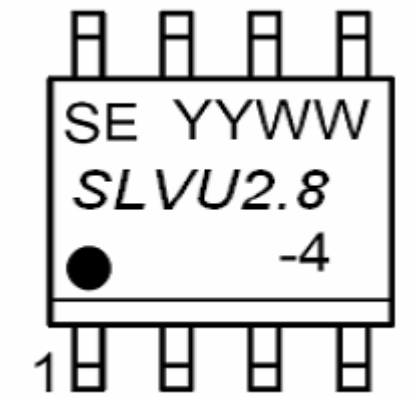
SLVU2.8-4 Utralow Capacitance Transient Voltage Suppressors Array

Features

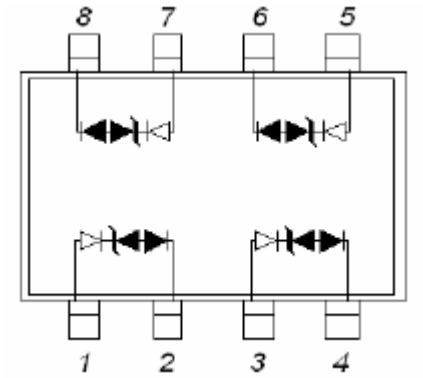


SOP-8

- 400 W Peak Pulse Power per Line (tp=8/20μs)
- Protects two line pairs(four lines).
- Low capacitance
- Low Leakage Current.
- Low Operating and Clamping Voltages.
- Transient Protection for High Speed Data Lines to
  IEC61000-4-2(ESD)±15kV(air),±8kV(Contact)
  IEC61000-4-4(EFT) 40A(5/50ns)
  IEC61000-4-5(lightning) 24A(8/20us)

General Description

The SLVU2.8-4 is in an SOP-8 package and may be used to protect two high-speed line pairs.The “flow-thru”design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the SLVU2.8-4 minimizes the stress on the protected IC.



Applications

- Ethernet – 10/100/1000 Base T
- WAN/LAN Equipment

Desktops,Servers,Notebooks & Handhelds,base stations Laser Diode Protection

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Peak Pulse Power (t_p = 8/20μs) - See Fig1.	P_{PK}	400	W
Peak Pulse Current (t_p = 8/20μs)	I_{PP}	20	A
Storage Temperature Range	T_{STG}	-55 to 150	°C
Operating Junction Temperature Range	T_J	-55 to 150	°C

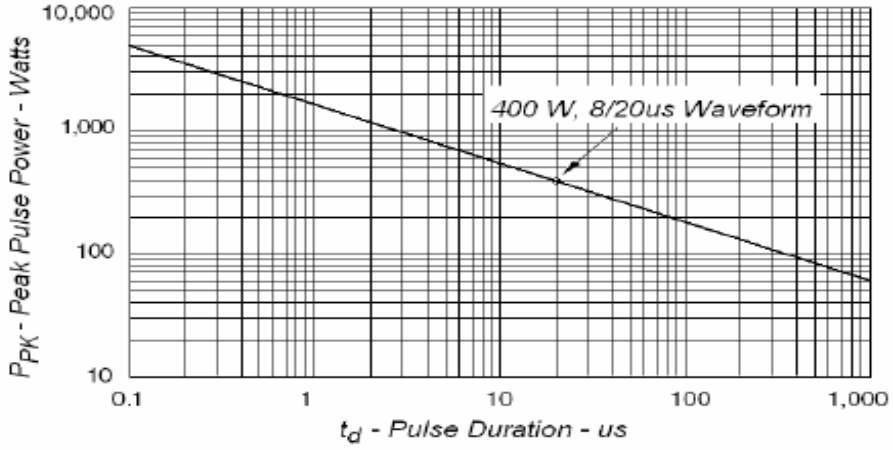


Fig1. Peak Pulse Power VS Pulse Time

Electrical Parameter

Symbol	Parameter
I_{PP}	Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse Stand-Off Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{SB}	Snap-Back Voltage @ I_{SB}
I_{SB}	Snap-Back Current
V_{PT}	Punch-Through Voltage
I_{PT}	Punch-Through Current
V_{BRR}	Reverse Breakdown Voltage @ I_{BRR}
I_{BRR}	Reverse Breakdown Current

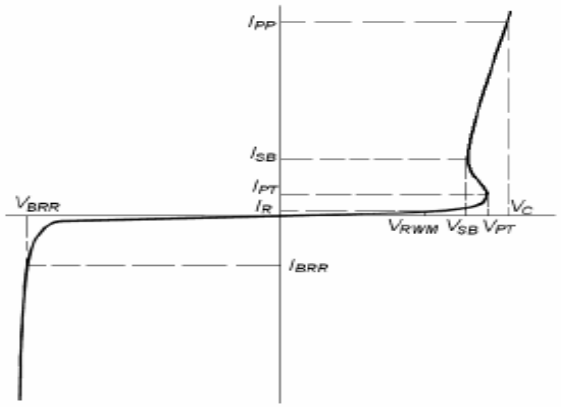


Fig2.

Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				2.8	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2uA	2.8			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} =2.8V, T=25℃ (Each Line)			1	uA
Clamping Voltage	V_C	I_{PP} =2A, t_P=8/20us (Each Line)			5.5	V
Clamping Voltage	V_C	I_{PP} =5A, t_P=8/20us (Each Line)			8.5	V
Clamping Voltage	V_C	I_{PP} =24A, t_P=8/20us (Each Line)			15	V
Junction Capacitance	C_j	VR =0V, f =1MHz (Each Line)		3.5	5	pF

Typical Characteristics

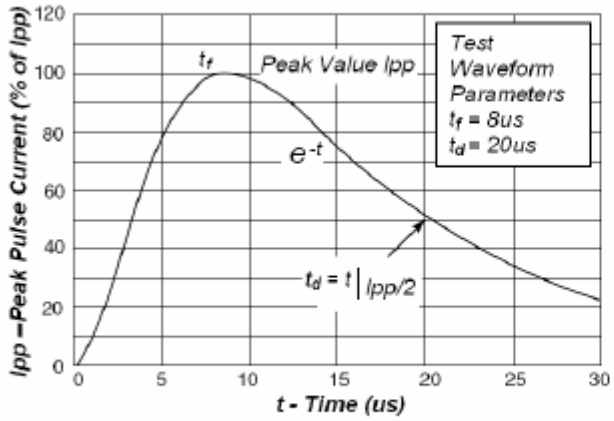


Fig3. Pulse Waveform

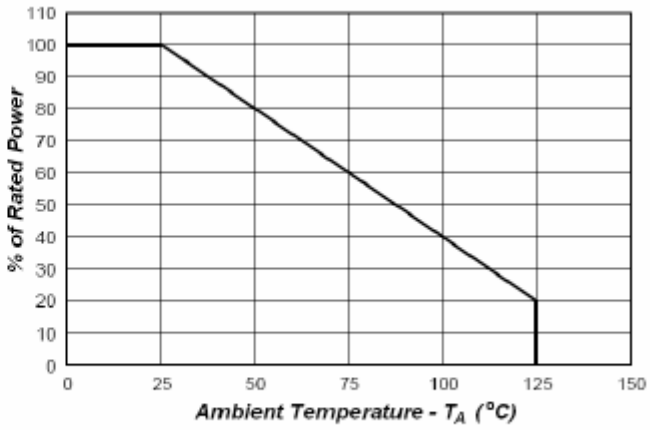


Fig4. Power Derating Curve

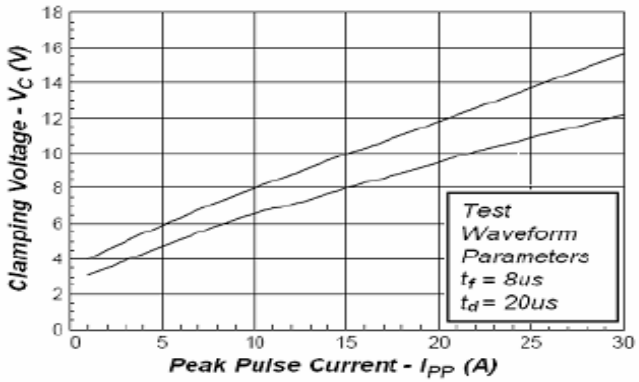


Fig5. Clamping Voltage vs. Peak Pulse Current

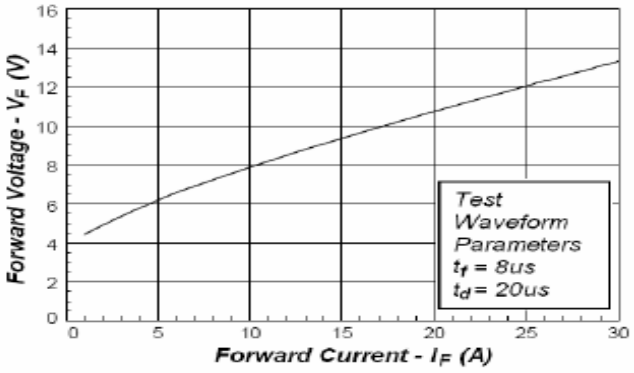


Fig6. Forward Voltage vs. Forward Current

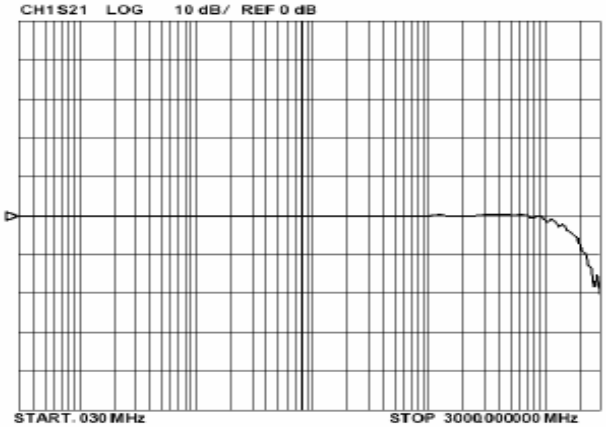


Fig7. Insertion Loss S21

Unidirectional Common-Mode Protection (Figure 9)

The SLVU2.8-4 provides up to four lines of protection in a common-mode configuration as depicted in figure 9. Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 7
- Line 3 is connected to Pin 3
- Line 4 is connected to Pin 5
- Pins 2, 4, 7 and 8 are connected to ground

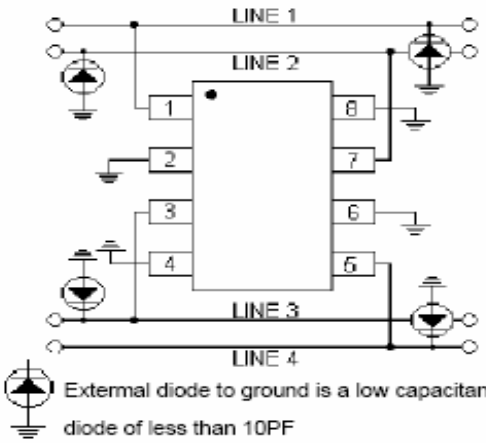


Fig9.

Bidirectional Common-Mode Protection (Figure 10)

The SLVU2.8-4 provides up to two lines of protection in a common-mode configuration as depicted in figure 10. Circuit connectivity is as follows:

- Line 1 is connected to Pins 1 & 8
- Line 2 is connected to Pins 4 & 5
- Pins 2, 3, 6, and 7 are connected to ground

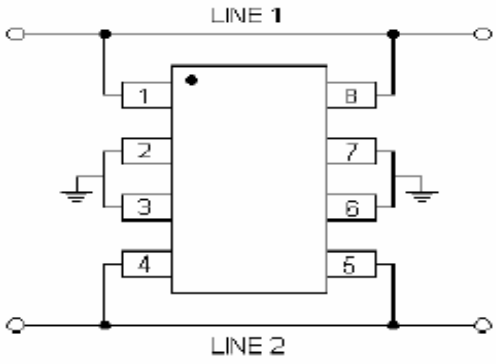


Fig10.

Bidirectional different-Mode Protection (Figure 11)

The SLVU2.8-4 provides up to two-line pairs of protection in a differenital-mode configuration as depicted in figure 11. Circuit connectivity is as follows:

- Line Pair 1 is connected to Pins 1 & 2
- Line Pair 1 is connected to Pins 7 & 8
- Line Pair 2 is connected to Pins 3 & 4
- Line Pair 2 is connected to Pins 5 & 6

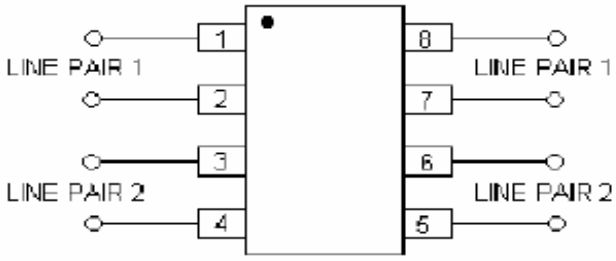


Fig11.

Circuit Board Layout Protection

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Typical Applications

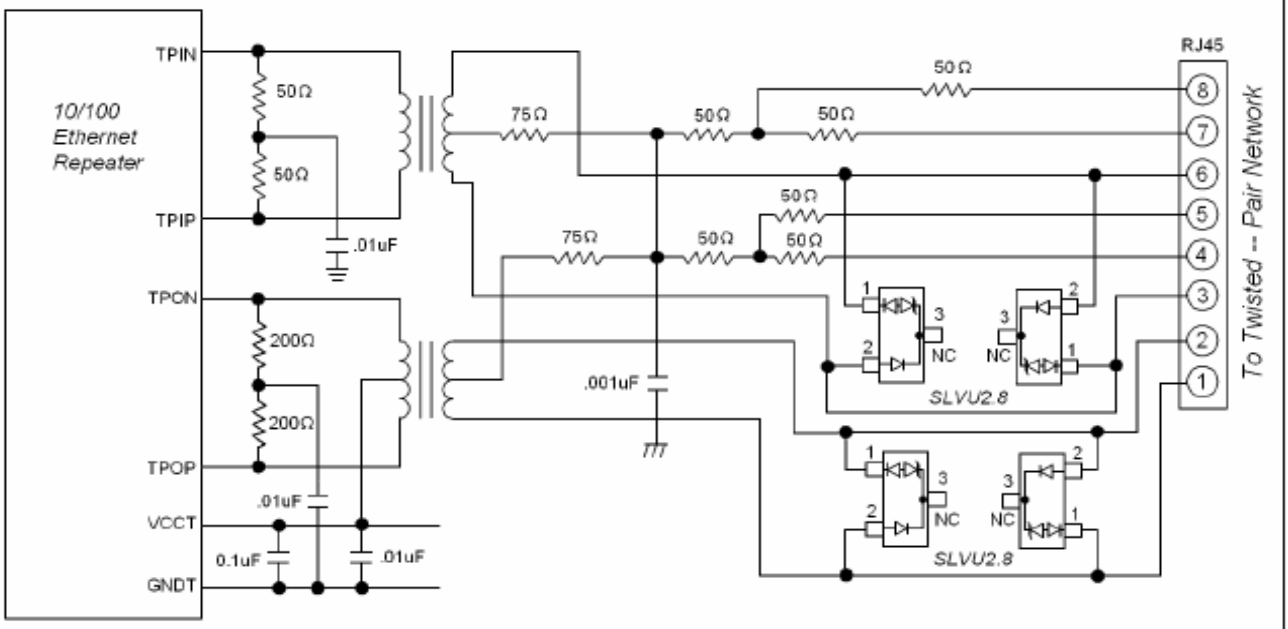


Fig12. 10/100 Ethernet Protection Circuit

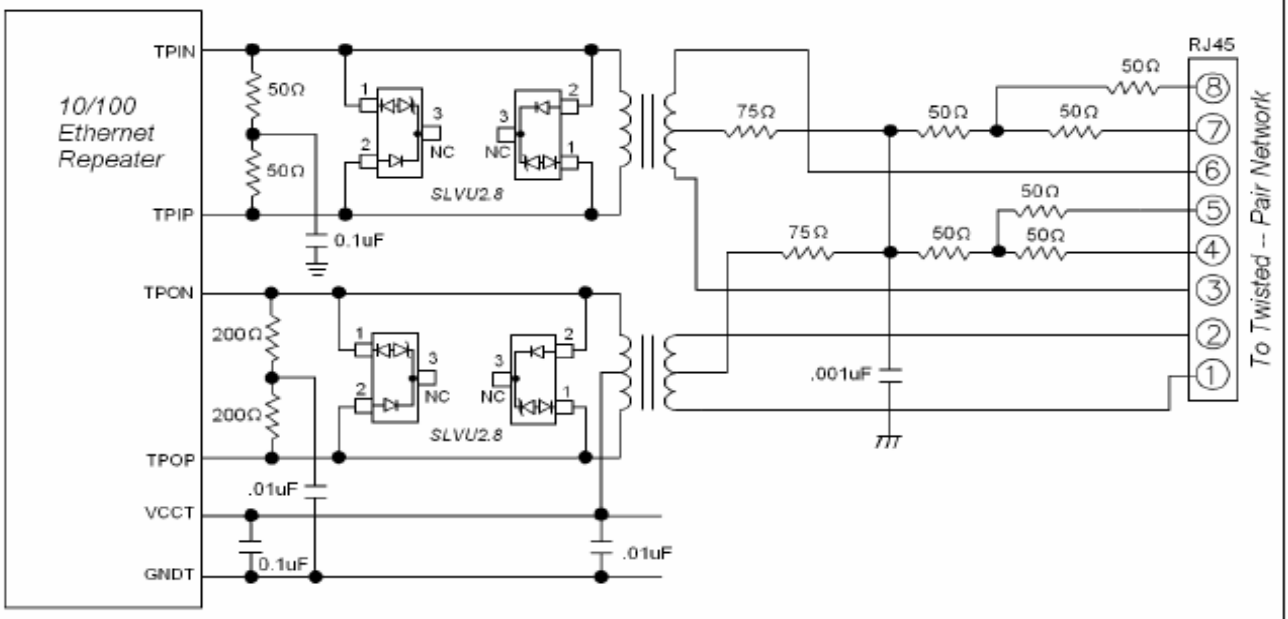


Fig13. 10/100 Ethernet "Enhanced" Lightning Protection Circuit

SOT-23 MECHANICAL DATA

Dim	Millimeters		
	Min	TYP	Max
A	1.00		1.40
A1	0		0.10
A2	1.00		1.30
b	0.35		0.50
c	0.10		0.20
D	2.70	2.90	3.10
E	2.40		2.80
E1	1.40		1.60
e	0.85		1.15
e1		1.90	
L1	0.40	.	
q	0°		10°
S	0.45		0.55